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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,438	BERNSTEIN ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 13-35 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 13-35 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 13-21,24, are rejected under 35 U.S.C. 102(e) as being anticipated by Parady (patent No. 6,295,600).

4. Parady taught the invention as claimed including a data processing ("DP") system comprising: multiple processing engines (32,34,36,38,40,42,44,46, see fig. 1) executing a least one instruction of a first thread having a first program counter[addresses in the program address registers](see. col. 3, lines 58-65), the at least one instruction including at least one instruction to issue request to a resource shared by the multiple processing engine (e.g., see figs. 1,2 and col. 3, line 8-col. 4, line 62);

5. Swapping execution to a second thread having a second program counter after processing engine execution of the at least one instruction to issue the request to the shared resource (e.g., see col. 4, line 3-col. 5, line 5); and

6. Swapping execution to the first thread after detection of a signal generated in response to the request to the shared resource (e.g., see col. 4, lines 52-62).

7. As per claim 14, Parady taught selecting a thread to executed by the processing engine (e.g., see col. 3, lines 7-col. 4, line 7).

8. As per claim 15, Parady taught the states comprising currently being executed by the engine (e.g., see col. 4, line 29-col. 5, line 5)[executing the thread before thread switch on blocking load or executing the load without thread switch on non-blocking switch], available for execution available for execution but not currently executing (e.g., see col. 4, line 9-col. 5, line 5)[using round robin thread switching threads wait their turn for execution]; waiting for detection of a signal before being available for execution [after memory access that caused thread switch the thread must wait until it is pointed to again by the round robin thread pointer to continue its operation] and wherein the selecting comprises a thread from among threads available for execution, but not currently executing (e.g., see col. 4, line 29-col. 5, line 5).

9. As per claim 16, Parady taught the selecting for thread comprises selecting the thread based on a round-robin among the threads available for execution (e.g., see col. 4, line 18-col. 5, line 5).

10. As per claim 17, Parady taught selecting the thread comprises selecting a thread other than the first thread after detection of the signal and before swapping execution to

the first thread (e.g., see col. 3, lines 7-col. 4, line 7)[using round robin selection select between four threads].

11. As per claim 18, Parady taught swapping execution comprises selecting a program counter associated with the selected thread (e.g., see col.. 3, line 58-65).

12. As per claim 19, Parady taught executing additional instructions of the first thread after the at least one instruction to issue the request to the shared resource and before swapping the first thread out[in one embodiment, on a non-blocking loads the system supports allowing the program to continue in the same program thread which memory access is being completed] (e.g. see col. 4, lines 63-66). ,

13. As per claims 20, 21,Parady taught executing instructions of a first thread explicitly requesting thread switching; and swapping execution to the second thread in response to the instruction explicitly requesting swapping (e.g., see col. 5, lines 6-53)[instruction that provides a conditional or unconditional jump to another thread], as per claim 21, Parady taught the instruction of the first thread explicit swapping does not comprise an instruction to issue a request to a shared resource (e.g. see col. 4, lines 63-66).

14. As per claim 24, Parady taught the shared resource comprising one of the following: a memory shared by the multiple processing engines internal to the processor and a memory shared by the multiple processing engines external to the processor (e.g. see fig. 1,2)[data cache(56) and L2 cache shared by the plural execution units] (32,34,36,38,40,42,44,46).

Claim Rejections - 35 USC § 103

15. Claims 22, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady (patent No. 6,295,600).

16. Parady taught the invention as claimed including a data processing ("DP") system comprising: multiple processing engines (32,34,36,38,40,42,44,46, see fig. 1) executing a least one instruction of a first thread having a first program counter[addresses in the program address registers](see. col. 3, lines 58-65), the at least one instruction including at least one instruction to issue request to a resource shared by the multiple processing engine (e.g., see figs. 1,2 and col. 3, line 8-col. 4, line 62);

17. Swapping execution to a second thread having a second program counter after processing engine execution of the at least one instruction to issue the request to the shared resource (e.g., see col. 4, line 3-col. 5, line 5); and

18. Swapping execution to the first thread after detection of a signal generated in response to the request to the shared resource (e.g., see col. 4, lines 52-62).

19. As per claims 22,23 Parady did not expressly detail at least one instruction identifies the signal. However since Parady taught a system where a L2 cache miss signal is received by thread switching logic and signals from thread switching logic are sent via a common line to the plural threads (e.g., see fig. 3) There it would have been obvious to one of ordinary skill that the instruction in a particular thread that was executing would have identified its signal since each thread is sent each thread switching logic signal (otherwise all the threads would not be independent). As the claim

is understood the instruction identifies the signal by instructing the apparatus to determine whether the proper signal was received acknowledging receipt of the request or indicating the thread was to be switched or not due to long latency in processing the request, and this was taught by Parady as discussed above.

20. Claim is 25 rejected under 35 U.S.C. 103(a) as being unpatentable over Parady as applied to claim 13 above, and further in view of Ramakrishnan et al (patent No. 6,085,215).

21. Ramakrishnan taught receiving a packet; and processing the packet using the first thread (e.g., see col. 9, lines 23-43, and col. 10, line 20-col. 11, line 47).

22. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Parady and Ramakrishnan. Both references are directed toward the processing of data in plural threads using round robin thread scheduling (e.g., see col. 11, lines 48-51 of Ramakrishnan. One of ordinary skill would have been motivated to add the Ramakrishnan teachings of receiving and processing packets using thread processing method and apparatus at least to provide a real world application for the thread processing of the Parady system (e.g., see col. 1, lines 10-33 of Ramakrishnan).

Claim Rejections - 35 USC § 103

23. Claims 26-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan (patent No. 6,085,215) in view of Parady (patent No. 6,295,600).

24. Ramakrishnan taught the invention as claimed including a data processing ("DP") system comprising:

a) Ethernet media access controller (e.g., see col. 2, lines 8-19); and

b) At least one network processor (28) communicatively coupled to the at least one Ethernet media access controller (e.g., see fig. 1) the processor processing multiple threads (e.g., see col. 7, line 53-col. 8, line 53) and interface (20) to the Ethernet media access controller (e.g., see fig. 1).

25. Ramakrishnan did not specify (claims 26,31) the internal configuration of the network processor that processed the multiple threads in real-time. Parady, however. taught a processor comprising multiple multithreaded processing engines (32,34,36,38,40,42,44,46)[note multiple threads for integer thread in integer register files in integer execution logic and multiple threads for floating point threads stored in FP register files in floating point execution logic in figure 3 and figure 5 (e.g., see col. 5, lines 16-28)],

26. Ramakrishnan taught memory internal to the processor shared by the multiple processing engines (L2 cache e.g., see fig. 2); at least one interface to the at least one memory external to the network processor (cache control system/interface 22).

27. Ramakrishnan did not specify (claim 26) that individual ones of the engines including an arbiter to select a thread to execute, however Parady taught grouping of the threads into a integer thread group stored in integer register files (48,158) and a floating point thread group stored in floating point register files (50,172) that are respectively executed on the integer execution logic and floating point execution logic (e.g., see figs. 3,5 and col. 5, lines 16-28). One of ordinary skill would have been motivated to include individual thread switching logic within the processing engines in at

least one implementation of the Ramakrishnan and Parady teachings at least to provide the system with the ability to efficiently perform thread switching when only one floating point unit and one integer unit were used for the plurality of grouped threads such as when the other execution logic was not operational or when to reduce system cost only one integer and one floating point unit was employed.

28. One of ordinary skill would have been motivated to combine the teachings sof Ramakrishnan and Parady. The incorporation of the specifics of the thread switching logic as taught by Parady would have allowed the Ramakrishnan system to efficiently implement the switching of thread in packet processing.

29. As per claims 27,32, Parady taught the states comprising currently being executed by the engine (e.g., see col. 4, line 29-col. 5, line 5)[executing the thread before thread switch on blocking load or executing the load without thread switch on non-blocking switch], available for execution available for execution but not currently executing (e.g., see col. 4, line 9-col. 5, line 5)[using round robin thread switching threads wait their turn for execution]; waiting for detection of a signal before being available for execution [after memory access that caused thread switch the thread must wait until it is pointed to again by the round robin thread pointer to continue its operation] and wherein the selecting comprises a thread from among threads available for execution, but not currently executing (e.g., see col. 4, line 29-col. 5, line 5).

30. As per claims 28,33, Parady taught the selecting for thread comprises selecting the thread based on a round-robin among the threads available for execution (e.g., see col. 4, line 18-col. 5, line 5).

31. As per claims 29,34, Parady taught swapping execution comprises selecting a program counter associated with the selected thread (e.g., see col.. 3, line 58-65). Therefore in the implementation with an individual arbiter internal the each execution unit one of ordinary skill would have been motivated to has the individual processing engines use a program counter associated with the thread selected by the processing engine's arbiter since the arbiter would have been readily available.

32. As to claims 30,35, Parady taught executing instructions of a first thread explicitly requesting thread switching; and swapping execution to the second thread in response to the instruction explicitly requesting swapping (e.g., see col. 5, lines 6-53)[instruction that provides a conditional or unconditional jump to another thread].

Response to Arguments

Applicant's arguments with respect to claims 13-35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sharangpani (patent No. 6,272,520) disclosed a method for detecting thread switch events (e.g., see abstract).

Dobbins (patent No. 5,485,455) disclosed a network having secure fast packet switching and guaranteed quality of service (e.g., see abstract).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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